

1. [6 pt] What type of hardware support is required to implement cycle stealing?

2. [6 pt] Explain why does the use of DMA result in the CPU memory accesses to slow down?

3. [6 pt] What is the difference between synchronous and asynchronous interrupts? Given an example of each of them.

4. [6 pt] Two processes execute the following command on the semaphore `mutex` concurrently:

```
signal ( mutex );
```

What will be the effect of the concurrent signal on `mutex` by those two processes?

5. [6 pt] Explain what happens during a context switch by enumerating the steps starting from the cause to the completion.
6. [6 pt] We described a few algorithms for mutual exclusion (for example, the hardware-based solution) where we suggested that we may not have the bounded-wait condition for our protocol to be satisfied. Yet, we said that we'll be satisfied with the solution. Why?

7. [8 pt] We added two states – “Blocked Suspended” and “Ready Suspended” in our process state transition model. Explain the need for those two states. How do the different states in our model compare with the process states in Linux?