Computer Organization & Architecture Fall 2002

Test 3 Max Pts: 48

Important: This is an open book test. You can use any books, notes, or paper, but not exchange anything with other students. You are not allowed to use any electronic/communication devices. *Do not log into the computer during the test*. Any calculations and rough work can be done on the back side of the test pages. You will lose five points for not writing your name.

1. [6 pt] Show the contents of \$t0, \$t1, and \$t2 at the end of execution of following code. You must show all 32-bits.

2. [4 pt] Assume that an exception has occured in MIPS, possibly due to arithmetic overflow. How can you determine the address of the instruction that caused exception? Do you put this address in a general purpose register or in some other register? Explain your answer.

3. [6 pt] Show the contents of \$t0, \$t1, and \$t2 at the end of execution of following code. You must show all 32-bits.

4. [8 pt] Multiply 8_{10} by -6_{10} using Booth's algorithm.

5. [4 pt] Show the representation of 0.48×10^{-4} in binary.
6. [4 pt] What is the difference between a combinational element and a state element. Give an example
of each.
7. [4 pt] Why is single cycle implementation of CPU not very good in practice?

8. [8 pt] Let the operation time for major functional units in multicycle CPU be

Memory unit 2 ns
ALU and adders 2 ns
Register file (read or write) 1 ns

Let there be no delay in multiplexors, control unit, PC access, sign extension, and other wires. Assume a mix of instructions to be 23% loads, 10% stores, 40% ALU, 15% branches, and the rest jumps. What is the performance improvement when you go from single cycle to multicycle implementation?

9. [4 pt] In a number of instances using temporary registers, we seem to write into a register at the same time when we read from it. Does it cause a problem internally? Why not? What value of register will be read, the one in there already or the one being written in.